Chapter 15

Material-Integrated Sensing Systems

Integration of Sensing and Multi-Agent Systems in Materials and Technical Structures: Technological Aspects and Integration Technologies

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The technological aspects of data processing embedded in technical structures and materials is one major driving force of the distributed data processing methodologies and platforms investigated in this work. Material properties, actually available manufacturing technologies, impact of physical data processing units on material and structure properties, create hard constraints on the possible integration of data processing in such materials and the features of the data processing units. The following chapter outlines the state of the art of the integration of sensing systems in materials.

15.1 The Sensorial Material

The new paradigm shift of sensorial materials [BOS14G][LEH13] stands for the technology of sensing and the senses and will

- Support sensorization in diverse fields of use by providing pioneering technical solutions;
- Identify new areas of application for integrated sensors and develop practical implementation;
- Advance sensor integration to the level where sensor-equipped structures become sensorial materials;
- Perform fundamental and applied research and development to set new standards in safety, efficiency, robustness and reliability of technical products, and to enable new capabilities in fields like human-machine interaction.

The rise of sensorial materials is closely coupled to the migration from passive sensors to smart sensors integrating data processing and communication, shown in Figure *15.1*. This new concept integrates as much as possible functionality in materials, enabling distributed material-integrated sensor processing and transforming sensorial materials in perceptive distributed virtual machines. The main fields of application of sensorial materials are Load and Structural Health Monitoring.

As a concept, material-integrated intelligent systems have implicitly been around for quite some time. To a considerable degree, this is because the concept as such is not so much a human invention, but rather something that is deeply rooted in nature: The human skin and the human nervous system are the typical examples cited pertaining to material-integrated intelligent systems.

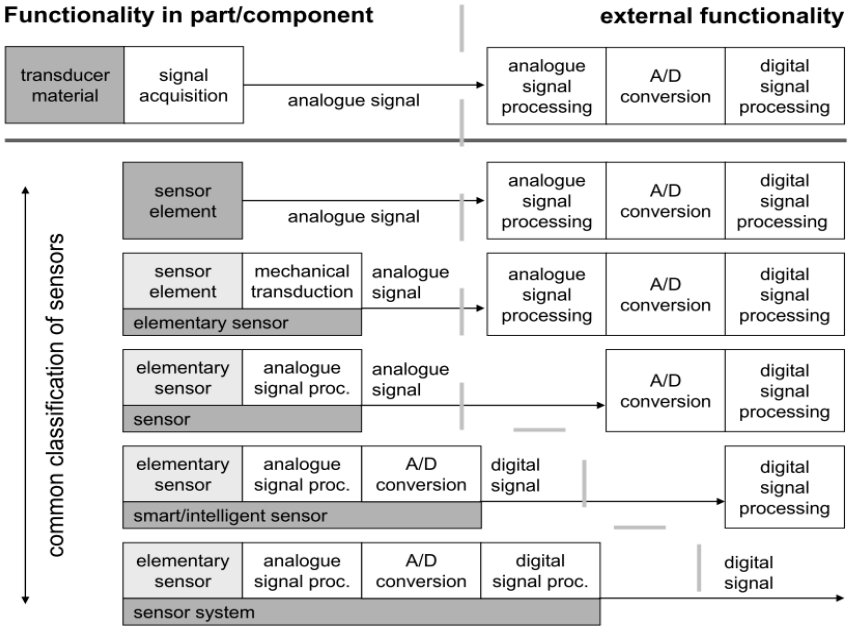

Fig. 15.1 *From passive Sensors to Smart Sensors and Sensorial Materials integrating the smart sensors in host materials and technical structures [from Diploma thesis of Sang Hyo Lee, 2010, University of Bremen].*

Having said this, we can derive a list of characteristics a material would need for us to concede that it can actually "feel." Such a material must be capable of

- capturing sensory data;
- aggregating data through some local preprocessing, performing data reduction of individual data points;
- further processing this data to derive some higher-level information, gaining knowledge;
- using this knowledge for decision-making, putting it to some internal/local use, or communicating it to higher system levels;
- coping with damage by being dynamic and reconfigurable;
- and achieving a state of awareness of host material and environment, that is, the derivation of a context knowledge.

15.2 Integration Levels

There are basically five different integration levels of sensing, illustrated in Figure *15.2*:

1. External applied sensing systems
2. Surface applied sensing systems (planar)
3. Surface integrated sensing systems (two-dimensional)
4. Volume integrated sensing systems (three-dimensional)
5. Intrinsic material properties: The material is the sensor, combined with levels 2-4.

15.2.1 Intrinsic Sensing Materials

Commonly intrinsic material properties derives some electric from mechanical characteristics, for example, the electrical conductivity depending on the stress (mechanical load) applied to a material.

Most material are not intrinsically perceptive. Common "sensorization" methods of materials are use the addition of conductive particles (discussed in detail in [WIE13]).

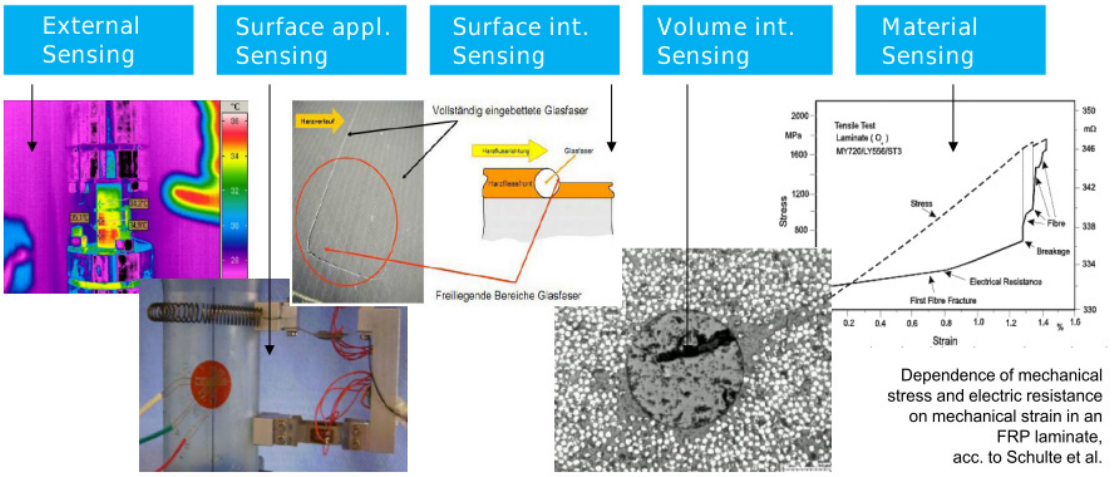

Fig. 15.2 *Different integration levels of sensing systems (Lehmhus, 2013, [MISS])*

15.2.2 Volume Integration of Sensing

The volume integration of sensing systems in materials, for example, part of technical structures like robotic actuators or wind power wings, can be classified in relation to the neighbour connectivity of sensors (sensor nodes) and their geometrical shape and arrangement, based on Newhams classification [NEW78] (first number: host-material, second number: sensor node), shown in Figure *15.3*, adapted by Lehmhus:

3-0

Individual sensor nodes with physical inter-connections, with network topologies in one, two, and three dimensions. The sensor networks can be considered as scattered point clouds (0D, for example, the Smart Dust Mote [WAR01]), line or fibre geometries (1D), areas (2D, smart path, functional net), or volumes (3D).

3-1

Sensor nodes are continuous in one dimension (wires, fibres,..)

3-2

Sensor nodes are continues in two dimensions, like functional nets or textiles

2-2

Layered material with full area smart layers of sensors

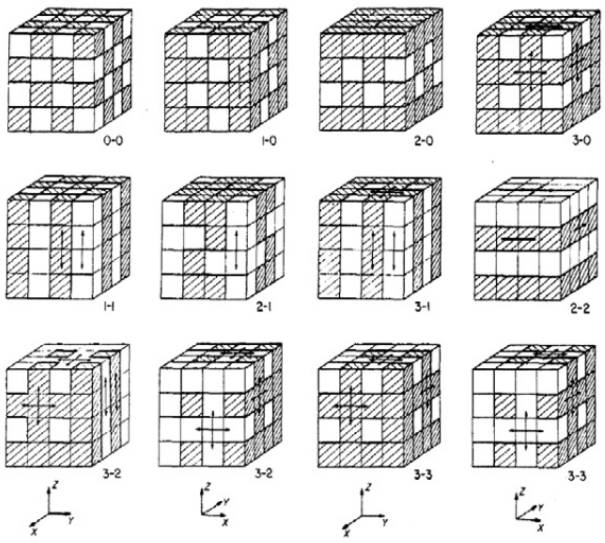

Fig. 15.3 *Classification of volume integration of sensing systems based on neighbourhood connectivity* [NEW78]

The major issues and challenged in the integration of sensor networks in materials can be summarized and classified by:

1. Mechanical stability
2. Thermal stability
3. Compatibility with the material matrix and the host material properties:
    - *i.* Mechanical matching (stiffness, flexibility, yield, ..)
    - *ii.* Thermal matching (thermal expansion coefficient)
    - *iii.* Chemical matching (reactivity, solution, ...)

3-0 Connectivity. An example for a 3-0 volume integration is a flat Si-based strain-gauge sensor that is a result of thinning and stripping processes, shown in Figure *15.4*. The carrier material (substrate) is a polyamide-metal-polyamide foil [LAN12]. This common sensor integration approach provides the sensor integration only, but no sensor signal processing, and no regular communication connectivity. The sensors are well suited for the embedding in fibre-like materials, like carbon- or textile materials.

The stripping and thinning of an original thick Si layer is called functional scaling that reduces a sensor or a microchip to its functional layer.

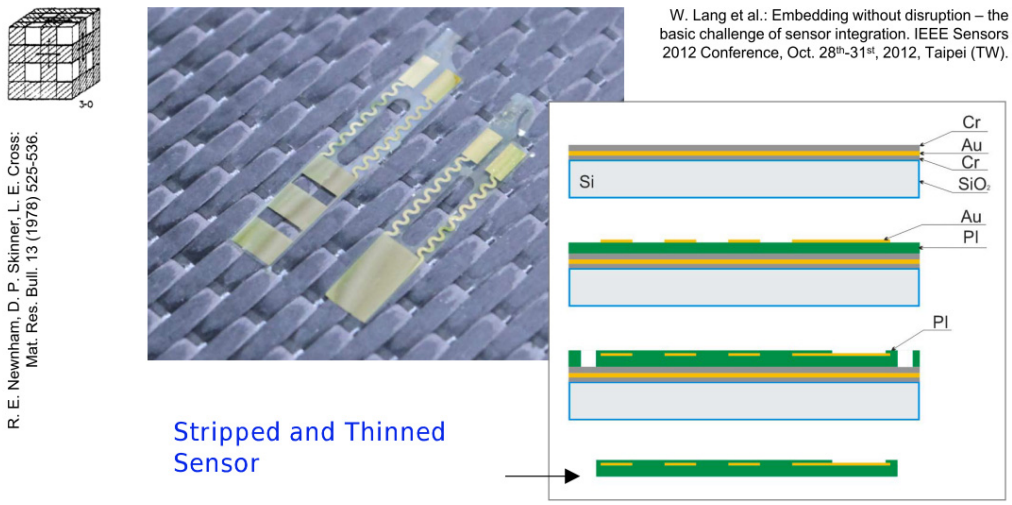

Fig. 15.4 *Si-based Strain-gauge Sensor resulting from thinning and stripping processes*

3-1 Connectivity. An example for a 3-1 volume integration is a chip-on-wire integration technology [BUL08], shown in Figure *15.5*. These sensorial wires can be directly embedded in fibre-like materials and sheet-layered materials. Furthermore, these wires can be easily molded in polymer-like materials.

2-2 Connectivity. An example for a 2-2 volume integration is a system-in-foil construction (a deeper discussion of this technology can be found in [DIE11]), shown in Figure *15.6*. The foil sheets are front and back cover materials that embeds the functional layer consisting of flat sensors, thinned Si-based [BUR11] or printed microchips, flat energy supplied and energy harvester (e.g., optical solar cells), and finally distributed communication infrastructures, which can provide the energy supply of sensor nodes, too (or only).

Volume integration of sensing systems can have disadvantages over surface integration or surface application. Volume-integrated sensing system can have significant impact on the mechanical structure properties, they are commonly not able to be serviced, and in load monitoring applications where the stress and deformation of the material that is sensed can be minimal (nearby the neutral area of the structure).

Further difficulties arise regarding the interconnect structures and their potential failure. This constraint can be minimized by using pure autonomous nodes with autonomous energy supply (energy harvesting) and wireless communication, referencing the Smart Dust Project and the Sensor Mote approach [WAR01].

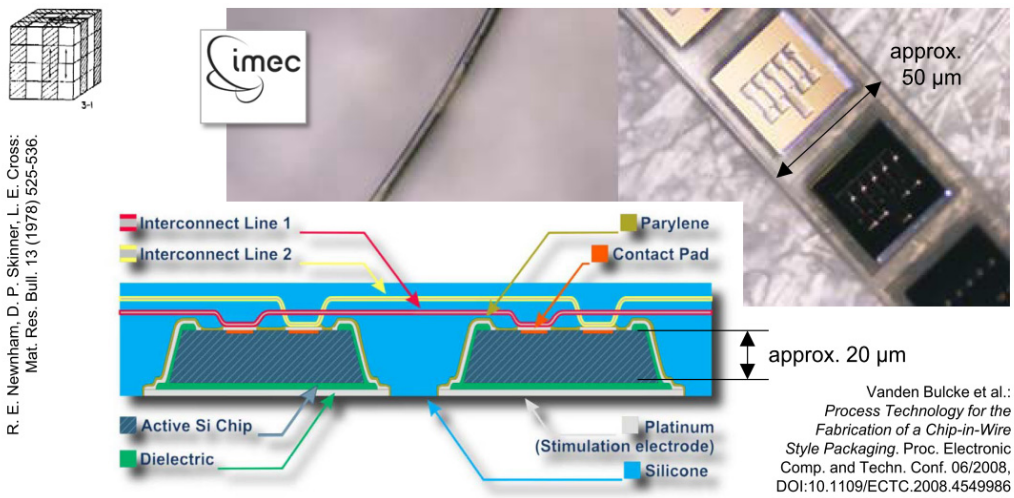

Fig. 15.5 *Chip-on-Wire: multiple active microchips are arranged along a line connected with a two-wire communication bus [IMEC, Belgium].*

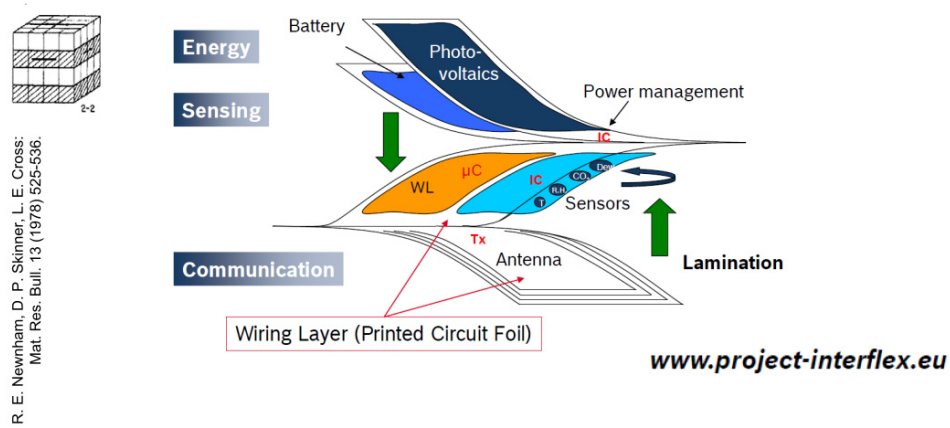

Fig. 15.6 *Planar foil-to-foil integration of sensors, data processors, energy supplies, and communication.*

But this approach is limited to non-conductive and basically non-dielectric host materials. And in the case of light-based wireless communication the host material must be transparent.

Volume- and surface integrated sensing systems undergo a higher failure rate, which can be compensated by increased system robustness using the self-organizing mobile agent approach discussed in this work.

15.2.3 Surface Integration of Sensing

Sensing systems can be more easily integrated in the surface of materials and technical structures compared with the volume integration. Laminating fabrication processes eases the integration significantly without disturbing the mechanical properties of the host material and the structure under test (SUT).

15.2.4 Surface Application of Sensing

The surface application is a still commonly deployed sensing application process that uses commonly discrete sensors glued or attached to the surface of the device under test.

15.3 Integration Technologies and Sensorial Materials

The major issues of integrating sensing systems in materials are related to the mechanical properties of the sensors, the electronics, and the interconnect technology. Concerning the mechanical properties of materials different

physical effects and loadings must be distinguished, which can select or limit suitable integration technologies, too:

- Flexibility versa Stiffness; Fracture caused by
- Stretch and/or
- Bend

Different geometrical structures can improve the capabilities of sensors, electronics, and connection structures to withstand loadings resulting in stretching or bending, shown in Figure 15.7. Complex geometrical structures and/or hybrid structures can result in complex deformations even under linear and in-plane loadings, i.e., mesh-like geometrical structures.

The integration of sensing systems and distributed sensor networks in materials and technical structures addresses multiple processing and integration technologies.

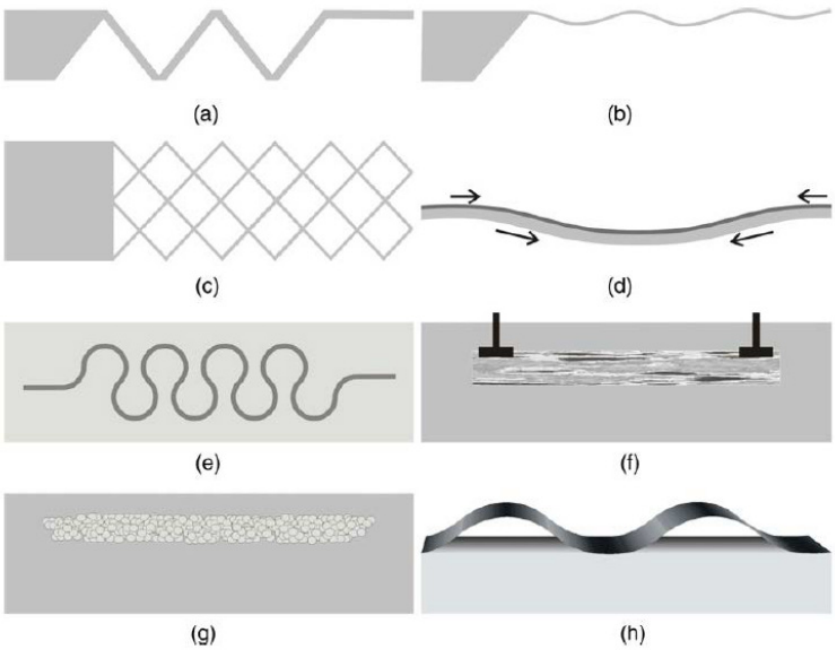

Fig. 15.7 *Examples of manufacturing technologies creating functional structures that can withstand stretch and bend* [LAN11].
(a) etched Si triangle wave structure (b) sine wave structure (c) etched Si two-dimensional mesh (d) metal layer on stretched Si (e) meander geometry on Polydimethylsiloxan/PDMS substrate (f) implanted gold cluster in Si substrate (g) liquid indium on PDMS (h) wave structure of Si

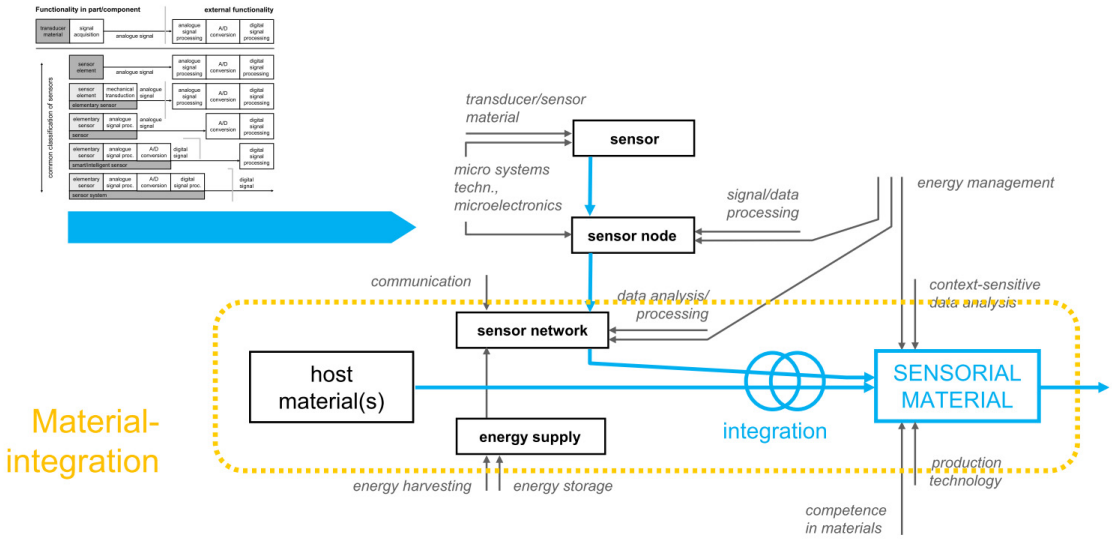

Fig. 15.8 *Material integration of sensing functions includes embedding of sensor nodes and sensor networks in host materials creating a sensorial material* [LEH13]

Different functional components must be integrated that rely on different materials having different mechanical and physical properties:

- Sensors
- Digital Electronics and mixed signal analogue/digital electronics
- Power supply and power electronics
- Energy storage
- Energy Harvester
- Interconnect Structures (wired, wireless, optical, electrical)

Material integration of sensing enables a functional integration, mainly sensor processing, communication, and information inference, creating a sensorial material, shown in Figure *15.8*.

15.3.1 Monolithic Integration

System-on-Chip (SoC) and Micro-Electro-Mechanical System (MEMS) designs offer an integration of sensors and sensor processing circuits on one microchip, either monolithic (one fabrication process) or with a hybrid approach, composing a MEMS of parts using different fabrication processes.

Today commonly the Silicon-on-insulator (SOI) technology is used to fabricate integrated circuits. The SOI technology processes achieves a minimal physical length below 100nm, advanced processes claim sizes below 20nm.

15.4 Digital Logic Technologies

The deployment of digital logic enables the optimized application-specific design and implementation of various data processing architectures far beyond traditional generic microprocessor system, though they are commonly implemented with large-scale digital logic, too. Digital logic itself is inherently parallel. But a parallel system usually requires synchronization for resolving competition (due to concurrent access of shared resources) and providing coordination. The multiprocess model introduced in Chapter *5* offers such coordination and can be immediately transformed to digital logic systems using Register-transfer architectures, briefly discussed in the next subsection.

15.4.1 Register-Transfer Architecture

The Register-Transfer Level (RTL) architecture decomposes a traditional program flow in a control and data flow. The control flow is represented by a state diagram and implemented with a finite-state machine, consisting of a control state register, a state transition logic, and an output logic. The data flow is composed of registers storing intermediate or final results of expressions, functional operators like arithmetic units performing the computation, and finally data path flow selectors (multiplexer and demultiplexer), required if resource sharing will be exploited, shown in Figure *15.9*. The RTL architecture is a base for different technological implementations discussed in the next subsections.

The data path is controlled by a Finite State Machine (FSM), that activates registers, selectors, and operational units depending on the current control state. The control signals are generated in an output logic (Π). The next control state is computed by a state transition logic (Σ), based on the current control state stored in register Z and input from the data path, too.

The state machine itself is an RTL architecture, too, with only one register, introducing some recursion of the architecture! The application-specific control and data path can be derived from a traditional program flow, discussed in Chapter *12*. The complexity of the RTL architecture depends strongly on the complexity of the algorithms to be implemented. Resource sharing like register merging in RAM blocks and state compaction can reduce the digital logic resources significantly, but large control state diagrams beyond 1000-10000 states are not very well suited for this architecture, which should be implemented preferred with program controlled machines (processors).

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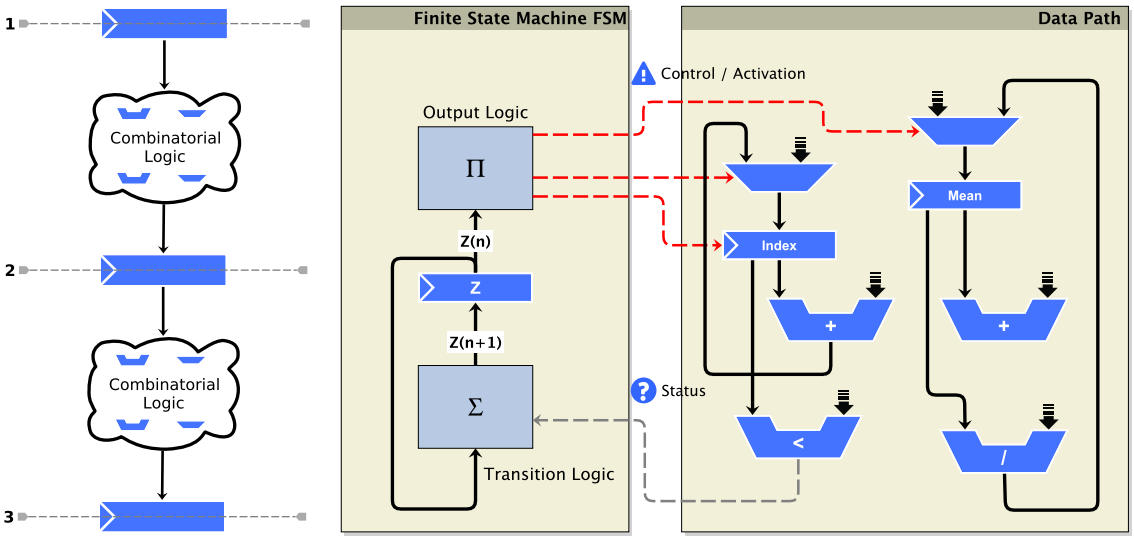

Fig. 15.9 *(Left) Principles of Register-transfer systems: computation by combinatorial logic is embedded between register layers. (Right) State-machine controlled data path*

Parallel execution of expression computations reduces the number of control states, but prevent resource sharing reducing the data path resource requirements.

It can be roughly estimated that the *PCSP* agent processing platform is suitable for an application-specific digital logic implementation with a few numbers of supported agent classes (less than 10) and if each agent class consists of less than 100 computation steps. The control path complexity of the *PCSP* platform increase with the number of supported agent classes and the computational complexity of the agents. In [BOS14A] the PCSP platform was implemented in an FPGA with about 1M equivalent gates, and for a hypothetical ASIC implementation the chip area was estimated below 10 mm^2. The programmable *PAVM* agent processing platform has a significant resource threshold caused by the processors, but the control path is nearly constant and independent of the number of agent classes and their computational complexity. Only the required RAM resources depend linearly on the number of supported agent classes and their complexity.

15.4.2 Semi- and Full-custom CMOS/Si-based ASIC Technologies

Today the Complementary Metaloxid Substrate (CMOS) technology is the prominent transistor architecture used for digital logic designs. A CMOS cell

consists of two complementary field-effect transistors (FET). A FET has the advantage being a voltage-controlled current source not requiring any additional components for the construction of digital logic cells (i.e., resistors or diodes), in contrast to bipolar transistors that are current-controlled current sources. Basic combinatorial logic gates can be easily implemented with CMOS cells [PDL], but the elementary CMOS cell is an inverter, hence all basic gates with the minimal number of transistors are inverting cells (NAND; NOR), as shown in Figure *15.10*. Commonly CMOS technologies are silicium-based, and a MOS transistor consists of either n- or p-doped silicium bulk material with embedded n+ or p+ doped buckets acting as the charge source (S) and drain (D). The gate (G) controlling the current flow between source and drain is attached by an insulation layer (SiO2) [WES05]. Sequential circuits like latches can be composed of combinatorial gates (inverters) with a signal back propagation and a multiplexer enabling the clock switching (activation).

Clock edge-triggered flip-flops can be composed by a combination of a positive- and negative-sensitive latch [WES05].

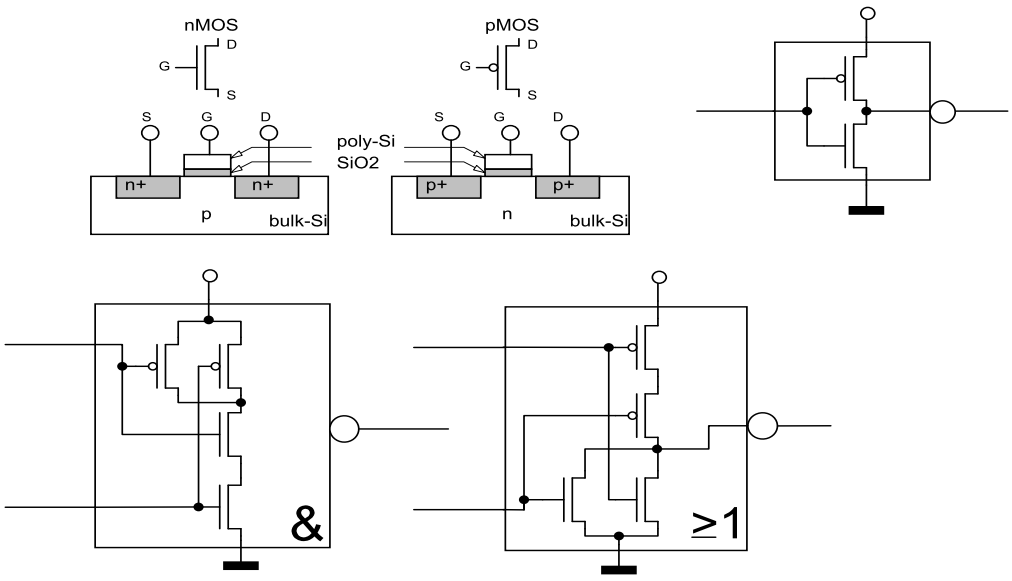

Fig. 15.10 *(Bottom, Right) Basic inverted digital logic gates (NOT, NAND, NOR) and their CMOS circuits consisting of paris of n- and p-type transistors. (Top) Cross-section view of transistor cells and circuit symbols*

The IC fabrication process requires clean-room conditions and is divided into multiple cycles of lithography, doping, and etching, as illustrated in Figure 15.11. Typical lost-cost processes reach transistor cell dimensions around 180nm, for example, the process technologies offered by TSMC within a wide range {250nm, 180nm, 130nm, 90nm, 65nm, 40nm}.

Full-custom ASIC technologies. They enable cutting edge designs with the best power and resources performances, but requires in-depth knowledge of electronics, physics, and a high degree of experience in the IC fabrication process. The designer specifies the transistor cell layout and composes logic cells on transistor level, finally composing the digital circuit.

Standard-cell ASIC technologies. In contrast, standard-cell approaches compose a digital logic circuit with pre-defined logic cells with already defined transistor layout. Commonly, standard-cell libraries are used already in several designs. This approach does not require in-depth knowledge of electronics and physics, easing the design process significantly and reducing the risk of failures.

Standard-cell libraries can be scaled with respect of the transistor size dimension (hence the fabrication process) on a large range. They offer the best economic solution for ASIC designs.

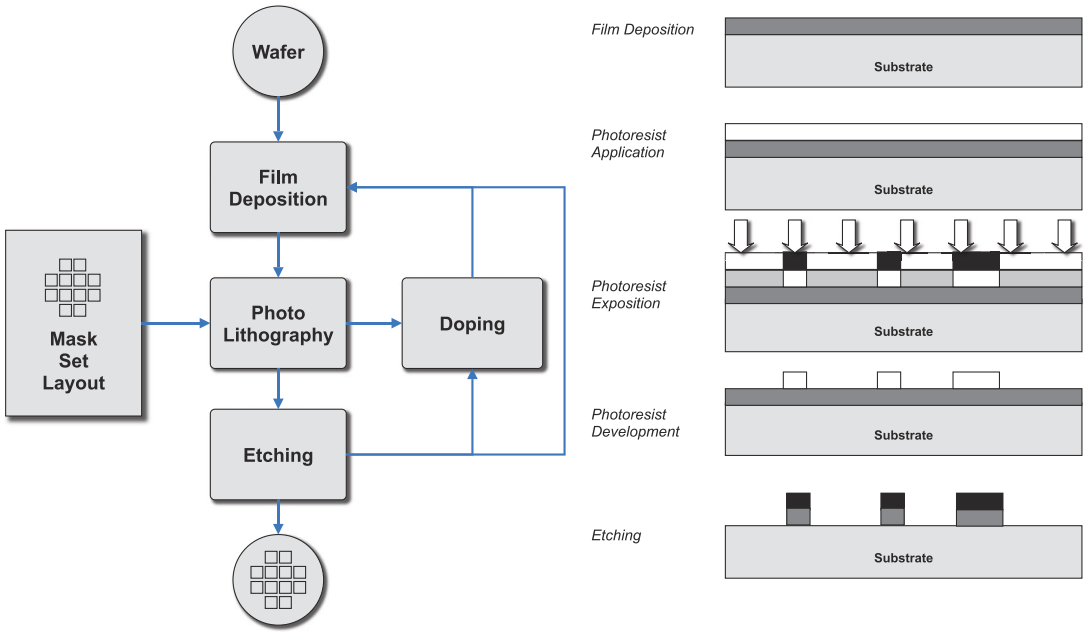

Fig. 15.11 *(Left) IC Fabrication Process (Right) Photolithographic Process and Etching*

15.4.3 Rapid Prototyping with FPGA Technologies

Due to the expensive and time-consuming ASIC fabrication process rapid prototyping process are very attractive, not only during the development phase of digital logic circuits, but also the deployment in the production phase of small-lot productions.

Programmable logic devices (PLD) base on an AND-OR plane structure composing combinatorial logic with product terms. One of the simplest PLD are RAM/ROM memories, shown in Figure 15.12. The static AND plane is related to the address decoder, and the programmable OR plane is related to the memory cell array [PDL]. The behaviour of a combinatorial logic can be specified using function tables mapping input variables on output variables. The output columns can be directly transferred to the memory cells, and the input variables. Further improvements can be achieved by replacing the AND plane with a reduced but configurable plane. The next evolution step was achieved by Complex PLDs that decompose a large block in simpler blocks.

These blocks are connected by an on-chip network (mesh-like interconnect network topology). CPLD introduce additional configurable register resources required for the implementation of sequential logic.

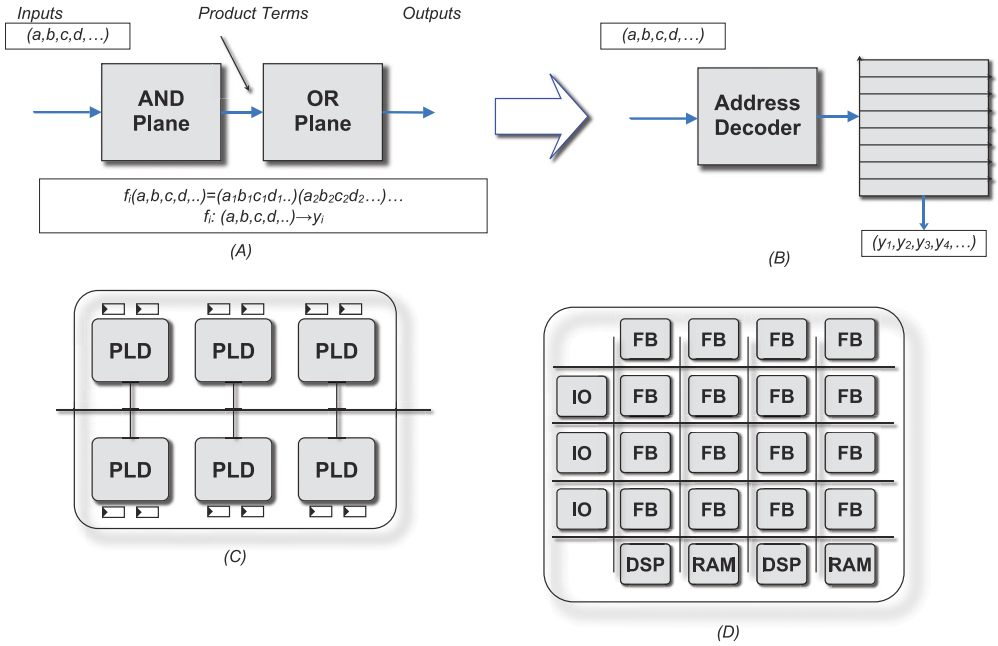

Fig. 15.12 *From Boolean Logic (A) to Programmable Logic Devices: (B) RAM/ROM based PLD (C) Complex PLD with configurable Registers (D) FPGA Architecture*

Finally, the Field Programmable Gate Arrays (FPGA) introduce an array of simple functional blocks, commonly using a small look-up table (LUT) to store small logic functions (around 2-4 input variables). A function block (FB) consists of the LUT RAM or ROM block, multiplexer, and register(s). A channel-based multi-stage interconnect network is used to connect the FBs with other FBs, Input-Output (I) blocks, and dedicated arithmetic blocks (DSP) or RAM blocks (RAM).

Compared with CPLDs, FPGAs offer a higher register density and logic gate equivalent counts beyond the Millions gate boundary [PDL]. FPGAs are well suited for complex logic designs, like the agent processing platforms *PCSP* and *PAVM* introduced in this book.

15.4.4 Printed and Organic Digital Circuits

Printed electronic bases on organic or metal transistor cells. They are commonly disposed with bubble-jet fabrication processes. Printed electronics and sensors have the advantage of low-cost fabrication processes compared with Si-based processes, requiring, for example, expensive clean rooms.

Printed electronics have the advantage of their mechanical flexibility and printed devices can be bent and partially stretched. Though Si-based microchips can be thinned and are flexible, too, but they can not be stretched. Both technologies and their fabrication processes are compared in Figure *15.13*.

Actually printed transistor cell dimensions in the millimetre range can be achieved [KLA12], compared with the sub-micrometer range of conventional semiconductor processes, and switching speeds in the upper microseconds range of printed transistors, compared with nanoseconds achievable in semiconductor devices.

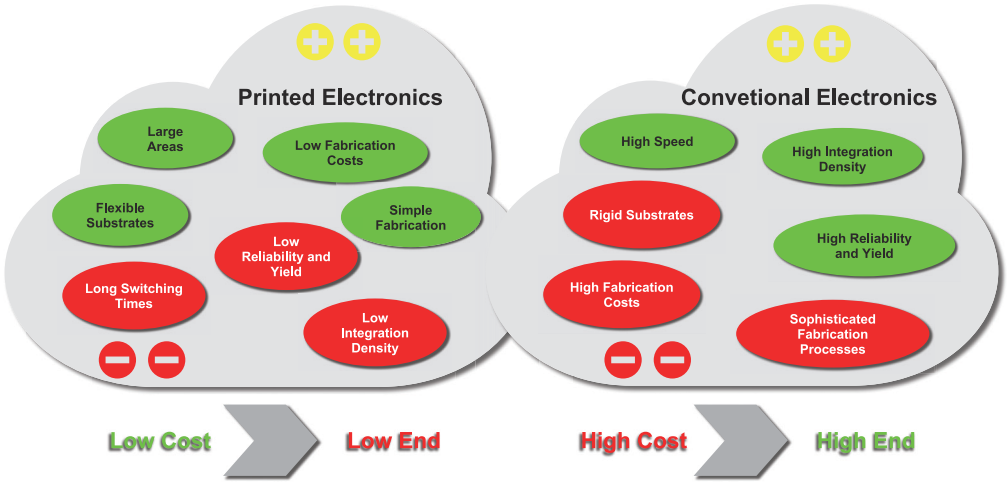

Fig. 15.13 *Comparison of printed and conventional semiconductor processes*

Due to the low integration density of printed digital electronics, the deployment of the low-resource and application-specific *PCSP* agent processing platform (see Chapter 6) is a possible suitable architecture candidate for this technology, but that can currently not confirmed.

15.5 Computational Constraints

Integrating computation in materials and structures requires a down-scaling of established algorithms, computer architectures, and co-ordination principles. A mobile computer equipped with an Intel i5-2520M and 4GB DRAM requires roughly A=150 (CPU) + 500 (DRAM) mm^2=650mm^2 chip area, delivering C=50000 Million Integer Instructions per second (MIPS) computing power, but demanding about 35(CPU)+5(DRAM)=40W electrical power. Mid-scale computers, e.g., smart phones, are equipped with low-power devices, e.g., an ARM Cortex A9 delivering C=7500 MIPS, requiring only A=7mm^2 core chip area and P=2W power. A normalized ***computing power efficiency factor*** of a computer (considering only the data processing unit) can be defined by

$$\varepsilon = \frac{C}{AP} \tag{15.1}$$

and a relative down-scaling ratio factor is given by

$$s = \frac{\varepsilon_1}{\varepsilon_2} = \frac{C_1 A_2 P_2}{C_2 A_1 P_1} \tag{15.2}$$

A scaling factor $s \gg 1$ is desired. The down-scaling from an Intel i5 to an ARM Cortex is expressed in a scaling factor of about 50. Material-integrated computing systems limit the size of a computer to roughly 1mm^2 chip area to limit the mechanical impact of electronic components on the structure. An ATMEL *ATtiny* 20 micro-controller provides C=12MIPS and requires A=1mm^2 and P=20mW. Compared with an i5 this gives a scaling factor of s=63. To summarize, current low-price consumer electronics can deliver about 20MIPS/1mm^2 via a high scaling factor, while current leading edge digital technologies (TSMC 28nm process) expect 4M logic gates/mm^2, an estimated 1000MIPS/mm^2, and 5MBit SRAM/mm^2 (based on [LAP09]).

New trends in microelectronics pose 3D structuring of electronic devices, increasing the computational power and memory storage multiple times. The functional layer of a silicon die has a width about 10mm (e.g., extracted by chip thinning [PRI14]), delivering up to 1000 MIPS/mm^2 or 250MBit/mm^3 assuming a simplified functional-interconnect-isolation layer sandwich structure.

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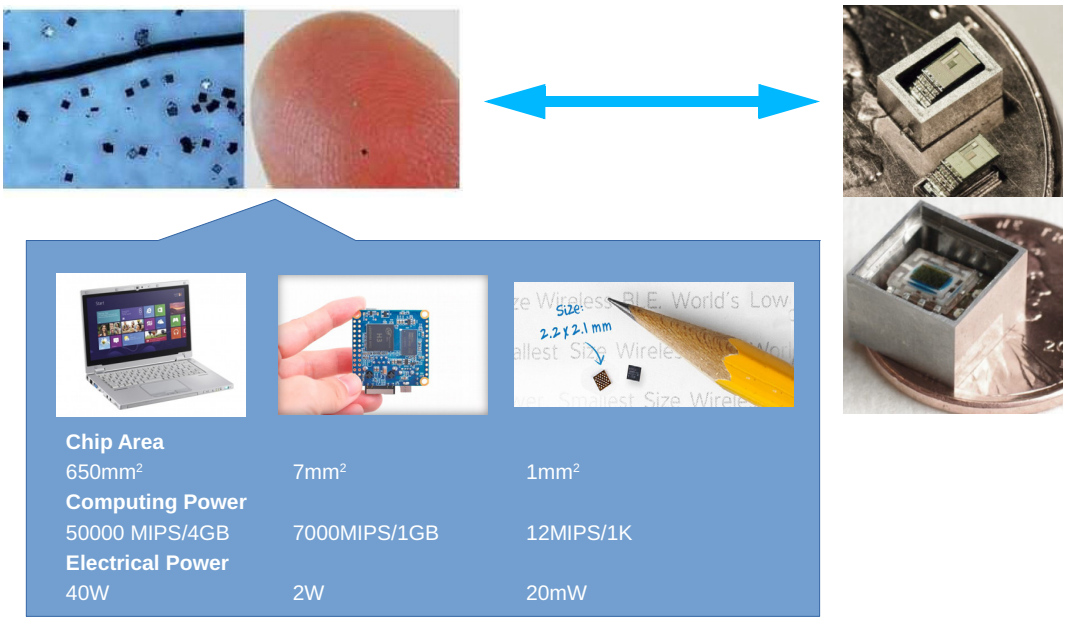

Fig. 15.14 *The Scaling Issue towards material-integrated computing (Left) Smart Dust (Right) Mote M3 & ELM* [CHO17]

The following Table *15.1* shows that the miniaturized ICT and sensor parts are already existing that enables material integration. The M3 Micro Mote delivers the best computing efficiency, followed by the Freescale KL03 (but lacking energy, sensors, and communication modules).

Large-scale sensor and data processing in networks embedded in materials, constituting material-integrated intelligent systems with thousands or millions of computers constrained by size below $1mm^3$ (e.g., Smart Dust, see Figure *15.14*) and low-power is a processing and moreover organisational challenge. Traditional Information-Communication-Technologies (ICT) fail! related to robustness, self-* features, and solving the organizational challenge. Artificial Intelligence (AI) methods can solve the scaling issue as outlined in this book, requiring a scaling of algorithms and architectures towards the design of distributed embedded systems, consisting of:

Up-scaling. Effecting the Speed-up (i.e., parallel performance) of parallel programs with respect to the number of nodes *N* and the data size *S*;

Down-scaling. Effecting Algorithms, their sequential performance and the deployment on embedded systems under hard low-resource constraints.

Platform / Property	*Michigan Micro Mote (M3)*	*ELM System*	*Atmel Tiny 20*	*Freescale KL03*	*ARM Cortex Smart Phone*
Processor	Arm Cortex M0	C8051F990 (SL)	AVR	Arm Cotex M0+	Arm Cortex A9
Clock	740kHz max.	32kHz	-	48MHz	1GHz
CPU Chip Area	0.1mm^2	9mm^2	1mm^2	4mm^2	7mm^2
RAM/ROM	3-4kB	0.5kB/2-8kB	-	2kB/40kB	512MB/4GB
Sensors	Temperature	-	-	-	Temp. , Light, Sound, Video, Accel., 3D Position, GPS, Magnetic, Air pressure
Communication	900MHz radio, optical	optical	electrical	-	3G/4G, WLAN, USB, Bluetooth, NFC
Harvester/ Battery	Solar cell/ Thin film	Solar cell/ Coin	-	-	-
Power Consumption	70μW / CPU	160μW / CPU	20mW	3mW @ 48MHz	100mW avg., 2W peak @ 1.5GHz
Manufacturing process	180nm CMOS	-	-	-	40nm CMOS
Package	Wire bonded Silicon Stack	PCB	Single Chip	Single Chip	PCB
Computing Eff. ε	***150***	***0.02***	***0.6***	***4.0***	***0.53***

Tab. 15.1 *Comparison of different ICT Hardware Platforms (Sub-micro computers) suitable for Smart Materials compared with a smart phone system (M3/ELM data from* [CHO17]*)*

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15.6 Further Reading

1. S. Bosse, D. Lehmhus, W. Lang, M. Busse (Ed.), *Material-Integrated Intelligent Systems: Technology and Applications*, Wiley, ISBN: 978-3-527-33606-7 (2018)
2. R. S. Dahiya and M. Valle, *Tactile sensing arrays for humanoid robots*, in Research in Microelectronics and Electronics Conference, 2007. PRIME 2007
3. R. S. Dahiya and M. Valle, *Robotic Tactile Sensing - Technologies and System*, Springer, 2013, ISBN 9789400705784